IN THE SPECIFICATION

Page 1, before the first line, add the paragraph:

--This is a continuation application of U.S. Serial No. 09/961,250, filed September 25, 2001.--

Page 12, after line 14, add the following paragraph:

--Fig. 23 is a circuit diagram showing the relationship between an equivalent circuit of a conventional dual band type high frequency power amplifier module incorporating a GSM and a DCS and semiconductor chips and the like.--

Page 21, the second full paragraph (lines 10-23), amend the paragraph as follows:

It is one of the features of the invention that the gate electrodes (G) and drain electrodes (D) of the first ~~EFTs~~ FETS and second FETs are laid out such that they are alternately provided in the same direction. In such a layout, the direction of extracting the output of the first FETs (first amplifying stage) or the direction in which wires extend therefrom is not close and adjacent to the direction of extracting the output of the second FETs (second amplifying stage) or the direction in which wires extend therefrom (see Fig. 13), which makes it possible to present any reduction in

gain and isolation attributable to a mutual induction effect between the wires. That is, any reduction in isolation can be suppressed, and any reduction in gain attributable to a mutual induction effect between the wires can be prevented.

Pages 29-30, the paragraph bridging these pages from page 29, line 19 through page 30, line 9, amend the paragraph as follows:

During the fabrication of the HBT, etching is performed to form an isolation groove 76 in the n-type GaAs collector layer 67 and n^+-type GaAs sub-collector layer 66. The isolation groove 76 reaches the top of the semi-insulating GaAs substrate 65. A metal layer 77 is provided on the bottom of the isolation groove 76 as an etching stopper. A contact hole 78 is provided on the bottom surface of the semi-insulating substrate 65. The hole 78 is formed such that its bottom is defined by the ~~meta,~~ metal layer 77. The wiring metals 74 are electrically connected to the metal layer 77 through conduction wiring 79 filled in holes provided in the insulation film 72. An electrode 80 is also provided on the bottom surface of the semi-insulating GaAs substrate 65, and the electrode 80 is connected to the emitter electrode 73

through the metal layer 77 and conduction wiring 79.

Reference numeral 81 in the figure represents a resistor.